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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,095	10/01/2001	Francois Balay	Balay 2-1	4702

7590 01/21/2005

MANELLI DENISON & SELTER PLLC
7th Floor
2000 M Street, N.W.
Washington, DC 20036-3307

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,095	BALAY ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10-12,14-17,19-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,10-12,14-17,19-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 11 and 12 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11 and 12 are identical.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 8, 10-12, 15,17, 19-21, 24, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Tai et al. (Tai).

As broadly drafted, these claims do not define any structure that differs from Tai.

With regard to claim 1, Tai discloses a system for interconnectlng two or more computer bus architectures (shown generally at Fig. 8, for example), comprising: a first bus segment (segment 802, column 6, lines 43-64, for example) to transmit data

information, a first half bridge circuit (700, shown at Fig. 7, on segment 802 side) connected to said first bus segment (segment 802, column 6, lines 43-64, for example), said first half bridge circuit (700, shown at Fig. 7, on segment 802 side) comprising a first DMA circuit (704, Fig. 7); a second bus segment (segment 804, column 6, lines 43-64, for example) to transmit data information; a second half bridge circuit (700, shown at Fig. 7, on segment 804 side) connected to said first half bridge circuit (700, shown at Fig. 7, on segment 802 side), said second half bridge circuit (700, shown at Fig. 7, on segment 804 side) comprising a second DMA circuit (704, Fig. 7) and transferring data information between said first bus segment (segment 802, column 6, lines 43-64, for example), and said second bus segment (segment 804, column 6, lines 43-64, for example).

With regard to claim 2, it is clear that segment 802 is a PCI architecture bus.

With regard to claim 3, it is clear that segment 804 is a PCI architecture bus.

With regard to claim 6, the first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

With regard to claim 8, the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment (see at least column 6, lines 52-64).

With regard to claims 10-12, 15, and 17, it is clear that one using the system of Tai would have performed the same steps set forth in claims 10-12, 15, and 17. See discussion above.

With regard to claims 19-21, 24, and 26, see discussion above regarding claims 1-3, 6, and 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 14, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tai.

Tai, as discussed above, discloses the claimed invention. Tai does not disclose that the bus operating frequencies of PCI bus segment (802) and PCI bus segment (804) may be different. However, the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having different frequencies, since the Examiner takes Official Notice that the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al, and providing Tai with two PCI buses having different frequencies only involves ordinary skill in the art.

Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tai.

Tai, as discussed above, discloses the claimed invention. Tai does not disclose the use of 'field programmable" or FPSC for the PCI half bridges (700, Fig. 7). However, the use FPSC for PCI half bridge is old and well-known as evidenced by the acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies (previously cited under "relevant art"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use FPSC for PCI half bridge, since the Examiner takes Official Notice that the use of FPSC for PCI half bridge is old and well-known as evidenced by the acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies (previously cited under "relevant art"), and using FPSC for PCI bridges of Tai only involves ordinary skill in the art.

Claims 1-3, 6, 8, 10-12, 15,17, 19-21, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura.

With regard to claims 1-3, Nakamura discloses a system for interconnecting two or more computer bus architectures, comprising: a first bus segment (PCI primary 2) to transmit data information; a first half bridge circuit (15) connected to the first bus segment (2); a second bus segment (PCI secondary 4) to transmit data information; a second half bridge circuit (35) connected to the first half bridge circuit (15) and the second bus segment (4) for transferring data information between the first half bridge circuit (15) and the second bus segment (4). Further, in Nakamura, the backplane defining the serial transfer path (300) is readable as a so-called "common back plane."

With regard to claim 6, in Nakamura, the PCI clock signals 1 and 2 have the same frequency and are generated by independent clock signal oscillators. With regard to claim 8, in Nakamura, the bus interface of the first half bridge circuit (15) and the bus interface of the second half bridge circuit (35) recover a clock signal from, respectively the first bus segment (2) and the second bus segment (4). See at least claims 1 and 14. With regard to claims 10-12, 15, 17, and 18, it is clear that one using the system of Nakamura would have performed the same steps set forth in claims 10-13, 15, 17, and 18. With regard to claims 19-21, 24, and 26, see explanation above regarding to claims 1-3, 6, and 8.

Nakamura does not disclose the use of DMA in the bridges. As well-known in the art, Direct Memory Access (DMA) is used to control the memory system without using the CPU. On a specified stimulus, the module will move data from one memory location or region to another memory location or region. The DMA can be configured to handle moving the collected data out of the peripheral module and into more useful memory locations (like arrays). Only memory can be accessed this way, but most peripheral systems, data registers, and control registers are accessed as if they were memory. In particular, the use of DMA is old and well-known as evidenced by Tai (see above), Futral et al. and Bauman et al. (both are cited below as relevant art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide DMA for the bridges of Nakamura, since the Examiner takes Official Notice that the use of DMA is old and well-known, as evidenced by Tai (see above), Futral et al. and Bauman et al. (both are cited below as relevant art), for

controlling the memory system; and providing the bridges of Nakamura with DMA only involves ordinary skill in the art.

Claims 5, 14, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, as applied to claims 1-3, 6, 8, 10-12, 15,17, 19-21, 24, and 26 above, and further in view of the following.

Nakamura, as discussed above, discloses the claimed invention. Nakamura does not disclose that the bus operating frequencies of PCI bus (2) and PCI bus (4) may be different. However, the use of two PCI buses having different frequencies is old and well-known evidenced by at least Lange et al. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having different frequencies, since the Examiner takes Official Notice that the use of two PCI buses having different frequencies is old and well-known, and providing Nakamura with two PCI buses having different frequencies only involves ordinary skill in the art.

Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, as applied to claims 1-3, 6, 8, 10-12, 15,17, 19-21, 24, and 26 above, and further in view of the following.

Nakamura, as discussed above, discloses the claimed invention. Nakamura does not disclose the use of 'field programmable" or FPSC for the PCI half bridges (15) and (35). However, the use FPSC for PCI half bridge is old and well-known evidenced by the acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies

(previously cited under "relevant art"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use FPSC for PCI half bridge, since the Examiner takes Official Notice that the use of FPSC for PCI half bridge is old and well-known, and using FPSC for PCI bridges of Nakamura only involves ordinary skill in the art.

Claims 1-3, 10-12, 14, 19-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al.

With regard to claims 1-3, Lange discloses a system for interconnecting two or more computer bus architectures, comprising: a first bus segment (primary PCI 12) to transmit data information; a first half bridge circuit (126) connected to the first bus segment (12); a second bus segment (secondary PCI 14) to transmit data information; a second half bridge circuit (127) connected to the first half bridge circuit (126) and the second bus segment (14) for transferring data information between the first half bridge circuit (126) and the second bus segment (14). With regard to claims 10-12, 14, 18, it is clear that one using the system of Lange would have performed the same steps set forth in claims 10-14 and 18. With regard to claims 19-21, and 23, see explanation above regarding to claims 1-3. In addition, Lange et al. also discloses that the first half bridge segment (12) and the second half bridge segment (14) communicate with a high speed serial line protocol (see at least col. 5, lines 49-51).

Lange does not disclose the use of DMA in the bridges. As well-known in the art, Direct Memory Access (DMA) is used to control the memory system without using the

CPU. On a specified stimulus, the module will move data from one memory location or region to another memory location or region. The DMA can be configured to handle moving the collected data out of the peripheral module and into more useful memory locations (like arrays). Only memory can be accessed this way, but most peripheral systems, data registers, and control registers are accessed as if they were memory. In particular, the use of DMA is old and well-known as evidenced by Tai (see above), Futral et al. and Bauman et al. (both are cited below as relevant art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide DMA for the bridges of Nakamura, since the Examiner takes Official Notice that the use of DMA is old and well-known, as evidenced by Tai (see above), Futral et al. and Bauman et al. (both are cited below as relevant art), for controlling the memory system; and providing the bridges of Lange with DMA only involves ordinary skill in the art.

Claims 6, 15, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al., as applied to claims 1-3, 10-12, 14, 19-21, and 23, and further in view of the following.

Lange et al., as discussed above, discloses the claimed invention. Lange et al. does not disclose that the bus operating frequencies of PCI bus (2) and PCI bus (4) may be substantially the same. However, the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tai and Nakamura. It would have been obvious to one of ordinary skill in the art at the time the invention was

made to use two PCI buses having substantially same frequencies, since the Examiner takes Official Notice that the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tai and Nakamura; and providing Lange et al. with two PCI buses having substantially same frequencies only involves ordinary skill in the art.

Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al., as applied to claims 1-3, 10-12, 14, 19-21, and 23, and further in view of the following.

Lange et al., as discussed above, discloses the claimed invention. Lange et al. does not disclose the use of 'field programmable" or FPSC for the PCI half bridges (15) and (35). However, the use FPSC for PCI half bridge is old and well-known as evidenced by the acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies (previously cited under "relevant art"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use FPSC for PCI half bridge, since the Examiner takes Official Notice that the use of FPSC for PCI half bridge is old and well-known, and using FPSC for PCI bridges of Lange et al. only involves ordinary skill in the art.

Response to Arguments

Applicants' arguments filed 11/19/2004 have been fully considered but are moot in view of the above new grounds of rejections.

US Patent Nos. 6,081,851 to Futral et al. and 6,721,839 to Bauman et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner